parMERASA

Multi-Core Execution of Parallelised Hard Real-Time Applications Supporting Analysability

parMERASA use cases

The parMERASA project is the response to demands from European avionic, automotive and automation industries for increased performance at reduced costs while maintaining safety levels. Its aim is to stimulate industrial, social and environmental changes by demonstrating the benefits of moving from embedded single core to multi-core processors which can run applications in parallel, speeding up performance and cutting costs.

This brochure describes the intended use cases of the parMERASA project and answers the following questions in detail:

1. What is parMERASA?

2. Who are the parMERASA partners?

3. How will the findings from parMERASA be applied?

4. How will tool support be provided?

5. What impact is parMERASA expected to have?

1 What is parMERASA?

Increased performance at reduced costs while maintaining safety levels are the key demands from European avionic, automotive and automation industries. The latest state-of-the-art embedded single core processors cannot cope with these demands. The pursuit of higher performance, improved safety and lower costs requires a new solution.

The goal of the parMERASA project is to demonstrate the use of multi-core processors in real-time systems. To meet this goal, the project must overcome the problems of existing timing analysis approaches, which only cover sequential program execution (where instructions are carried out one after another on a single core processor – in sequence – and only one instruction may be carried out at any moment in time).

A software engineering approach will be developed to ease sequential to parallel program execution (where multiple program instructions are carried out simultaneously – in parallel – on many processors and in less time than with a single processor). Verification and profiling tools will also be developed to support parallelisation, and the project partners aim to provide recommendations to enhance automotive and avionics standards.

2 Who are the parMERASA partners?

The parMERASA project is driven by the future high-performance application demands of industrial partners and the needs of high profile key industrial end customers in the EU.

The industrial partners will provide suitable systems for parallelisation from their respective sectors (avionics – Honeywell International; automotive – DENSO AUTOMOTIVE Deutschland GmbH; and construction machinery – BAUER Maschinen). Rapita Systems will provide tools to support the parallelisation process, and will support multi-core architecture in its RapiTime timing analysis tool. The academic partners will contribute by their research knowledge in the areas of code parallelisation, WCET tools, real-time system software, and multicore architectures.

An Industrial Advisory Board (IAB) made up of high profile key industrial end customers from across the EU reinforces the project's industrial focus, and provides additional avenues for the dissemination and exploitation of results. Since some industrial partners and IAB members are already involved in standardisation activities such as AUTOSAR, the ISO 26262 automotive standard, and avionic IMA standard ARINC 653, the parMERASA project is also expected to contribute to the development of future standards.

3 How will the findings from parMERASA be applied?

Avionics

The avionics industry is experiencing ever-increasing demands for aircraft functionality and safety, requiring greater systems performance in both commercial and military markets. At the same time, there is pressure to reduce the size, weight and power requirements of on-board systems to reduce the aircraft's overall weight, with corresponding improvements in its fuel efficiency or payload capacity.

The results of the parMERASA project will contribute towards the development of future versions of avionics standards, permitting the use of multicore technology and parallelisation methods in future generations of aircraft.

Use case: collision avoidance algorithms

Honeywell International's path planning/collision avoidance algorithms can be parallelised and configured to evaluate the impact of different multi-core architectures. A typical environment for these algorithms is a computational grid consisting of 128 x 128 x 64 points, requiring approximately 170 million calculations for each frame update, with a minimum update rate of 1Hz.

Using a combination of multicore technology and parallelisation techniques, Honeywell International aim to decrease the overall execution time of each update cycle, permitting an update rate in excess of 10Hz.

Use case: stereo navigation algorithms

Stereo navigation algorithms have been used by a variety of ground vehicles to navigate in the absence of GPS. They have also been used in conjunction with GPS to determine vehicle rotational and translational changes (rates and velocities). A subset of the vision algorithms have also been used for collision detection.

Honeywell International has two classes of stereo navigation algorithms in development: SLAM (Simultaneous Localisation and Mapping) and RANSAC. Trials suggest RANSAC has a maximum update rate of about 0.6Hz, and initial estimates suggest that the SLAM algorithm will take approximately twice as long. Honeywell International aim to be able to run stereo navigation algorithms at 20Hz by exploiting the multi-core technology and parallelisation techniques developed during the parMERASA project.

Automotive

The automotive sector is also experiencing a considerable increase in the use of electronics and software to provide increased functionality and safety in automobiles. Key factors include cost reduction, reductions in fuel consumption, and additional safety features.

The parMERASA project will contribute to the development of future automotive standards and provide techniques and guidance for the use of multi-core technology in future generations of automobiles.

Use case: engine control

A typical engine controller consists of a number of tasks to be executed at the same time, with a combined code size in excess of 100,000 lines of code operating in a feedback loop. By parallelising the application, it is possible to increase the update rate of the feedback loop, leading to improved engine performance and greater fuel efficiency.

Preliminary investigations using dual-core systems for engine control have demonstrated that semi-automated parallelisation is possible. The high degree of parallelism in the parMERASA architecture, with up to 64 cores, will allow DENSO AUTOMOTIVE to devise a systematic approach for application parallelisation and explore the scalability and limits for massive parallel computing of hard real-time automotive applications.

Construction machinery

State-of-the-art construction machinery control software is exemplified by the large diameter rotary drilling rigs, hydraulic grabs, and slurry trench cutters produced by BAUER Maschinen. Control applications are increasing in complexity due to an increase in the level of automation, but also due to the addition of safety-related functions. As the complexity of control applications increases, the limits of sequential code will soon be reached.

Through parMERASA, an increase in the performance of control systems can allow the use of more efficient control algorithms, or provide the option of graceful degradation in the event of sensor failure, preventing costly downtimes.

Use case: construction machine control

Starting from the sequential control algorithm that is well known by the application engineers, BAUER Maschinen will parallelise a construction machine control application. BAUER Maschinen aims to show an increase in application performance by incorporating parallelisation of existing code, without requiring significant changes to the control algorithms.

4 How will tool support be provided?

New on-target verification tools are needed to understand the behaviour of the system and provide worst-case analysis, verification and profiling.

Rapita Verification Suite (RVS) tools from Rapita Systems Ltd reduce the cost of measuring, optimizing and verifying the timing performance and test effectiveness of critical real-time embedded systems in industries such as aerospace, automotive and construction. For this project, Rapita Systems Ltd will investigate tools and solutions for the verification needs of safety critical systems using multicore processors. In addition to providing tools to support the parallelisation and analysis of software using the parMERASA architecture, Rapita Systems will incorporate new parallel analysis techniques into its commercial verification tool suite – RVS – accelerating the impact on industry and providing an effective path to long term exploitation of the project results.

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5 What impact will parMERASA have?

This final section explores the impact of the parMERASA project on the companies involved and the wider scientific, economic and societal impact.

The overall technical objective of the parMERASA project is to achieve a breakthrough in techniques for parallelisation of industrial hard real-time applications, embedded multi-core processors, hard real-time support in system software for multi-cores, and WCET analysis and verification tools. This will make high-performance operations with time predictable execution of single or multiple threads on multi-core processors possible.

By promoting products and processes which tackle time-to-market and cost pressures:

- Honeywell International will be recognised as a leader in the research and development of emerging embedded multi-core systems;

- DENSO AUTOMOTIVE will gain from the potential of new tools and advanced architectures by reducing unit costs of production;

- BAUER Maschinen will produce faster automatic tools which will be driven by parallelised code;

- Rapita Systems will create and use state-of-the-art tools to penetrate further into the automotive and avionics markets.

parMERASA is also expected to provide at least four recommendations to either the AUTOSAR automotive standard or the IMA avionics standard, allowing those standards to be extended to take full advantage of parallel execution.

The parMERASA partners believe parallel execution and time predictability will have a significant impact on the development of transportation systems and industrial applications across Europe. Overall, the project is expected to reinforce the EC position in the field of safety critical computing systems and give European industry and academia an advantage in the highly competitive embedded systems markets.

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