



Multicore timing analysis solution *for aerospace*

- » Produce DO-178C/CAST-32A evidence
- » Evaluate multicore hardware
- » Optimize multicore code for timing performance

Multicore timing analysis

We provide a unique solution to support the use of multicore hardware in critical systems. This provides a path to DO-178C multicore certification to achieve CAST-32A objectives, reducing migration risks and opening up the benefits of increased performance available from using multicore hardware.

“Multicore systems are becoming more popular in critical embedded system development due to the increased performance they offer.

Our multicore timing analysis solutions solve an important challenge in using these complex systems; ensuring that the software execution time meets timing deadlines and satisfies certification objectives.”

Dr. Guillem Bernat, CEO of Rapita Systems

A unique solution

With the increasing adoption of multicore systems in the critical software industry, new methods are needed to analyze the timing behavior of these systems in line with DO-178C objectives.

Combining expert knowledge from dedicated engineers, products from groundbreaking academic research and industry-leading software tool support, our solution to multicore timing analysis is truly unique.

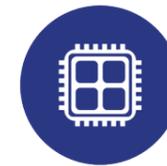
Use cases

Our solution supports a variety of use cases when migrating to, using and verifying multicore systems:



Produce certification evidence

Produce timing evidence for multicore systems to meet DO-178C and CAST-32A objectives.



Evaluate multicore hardware

Evaluate candidate multicore hardware architectures against performance criteria, taking into account the effects of contention from shared resources.



Optimize code for timing

Optimize multicore code for execution time behavior, ensuring it meets timing deadlines and can be verified against safety objectives.

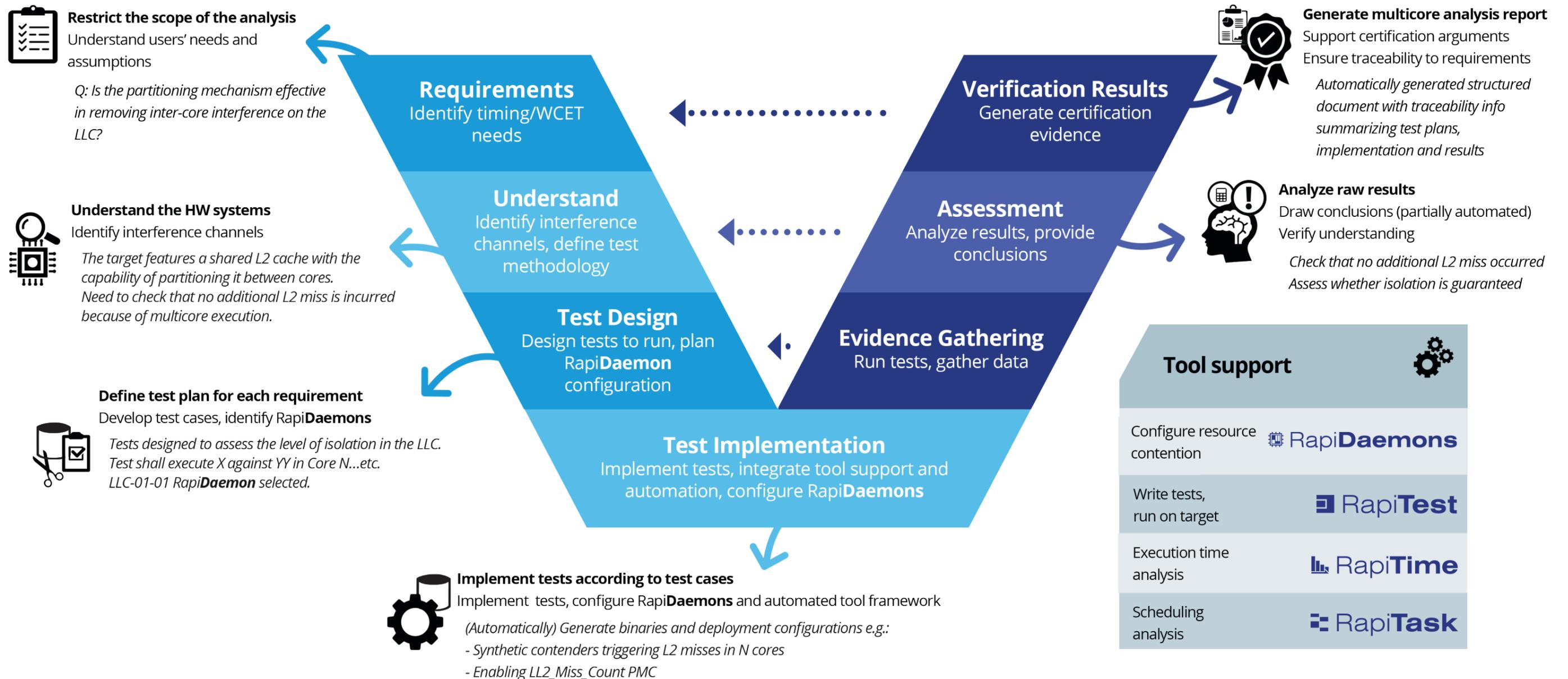
Benefits of our approach

Our approach not only identifies interference channels in multicore systems, but also quantifies them and takes them into account during timing analysis. We take advantage of industry-leading tool automation support to provide a cost-effective solution to analyze multicore timing behavior and produce timing evidence for DO-178C and CAST-32A certification of multicore systems.

Working with us

- We recognize that every project is different, and work with you to meet your needs.
- We run services at our engineering facilities in the UK or US. We can support projects with UK / US eyes only requirements.
- We can answer multicore timing questions and produce evidence for you, or implement a method and provide training so you can do so yourself.

How it works



Resource contention and interference

To analyze the timing behavior of multicore systems, the effects of *contention* on shared hardware resources such as caches and buses must be taken into account.

These effects generate *interference* that affects software execution time, and can in some cases have a huge impact. We determine the level of interference that can *realistically* occur in the system, as assuming the maximum level of interference possible leads to timing estimates that are wildly pessimistic and of no practical use.

RapiDaemons

To examine the effects of *resource contention* and *interference* on multicore timing behavior, our multicore timing services use RapiDaemons.

These are specially designed applications that can be integrated with the system under analysis to create a configurable degree of contention for shared resources such as caches and buses when running tests.

RapiDaemons are built on the Barcelona Supercomputing Center's (BSC) microbenchmark technology (MuBT).

*Meeting global testing needs in the critical
embedded software industry since 2004*

 Rapita location  Distributor  Customer



Get in touch

Each safety-critical project is different.
Contact us to arrange a custom solution that meets your needs:

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